Designing For Compliance 1999—Part 1: Know Partial Inductances to Control Emissions

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This is the first in our 1999 series of articles on designing for EMC compliance. We begin with the theory of partial inductances. These hold the key to predicting and mitigating emissions from digital devices.

No physical property of conductors has received, and deserved, more attention in recent years than the property of partial inductance. In this article we will explore what is meant by the term partial inductance and how according to the theory, it results in emissions from digital designs. Our future articles in this series will employ these theories to show how to substantially reduce emissions from almost any kind of device.

We will be relying heavily on two important papers. The first, "Identifying and Quantifying Printed Circuit Board Inductance" was presented at the IEEE Symposium on Electromagnetic Compatibility in 1994 by Todd Hubing, Thomas Van Doren, and James Drewniak of the University of Missouri at Rolla [1]. The second, published the following year, was a compilation of previous works on the subject by Frank Leferink entitled "Inductance Calculations: Methods and Equations" [2].

These articles both began with the classic definition of inductance. Inductance is defined as the ratio of magnetic flux that couples or passes through a closed path to the amplitude of the current that is the source of the magnetic flux. Mathematically: (1)

$$L = \frac{\Phi}{I}$$

Where:

L = Inductance in Henries

Φ = Magnetic flux through a closed loop

I = Current in the loop in Amps

Strictly speaking, inductance is only defined for complete loops. However, physicists have found it useful to assign a *partial* inductance to portions of a loop. The concept is illustrated in Figure 1. Current flowing in a loop creates a magnetic field passing through the surface bounded by the loop itself. That allows calculation of the loop's inductance from Equation 1. In order to assign a partial inductance to a portion of the loop, we can divide the loop into segments and, with a fair degree of physical accuracy, state that each segment has its own partial inductance. Adding the partial inductances of the segments together equals the total inductance of the loop itself.

For geometry such as a loop, the concept and calculation of partial inductance is trivial. However, for more complicated geometries, such as a trace lying over a finite plane, the calculation of partial inductances are anything but. Yet their precise calculation is of the utmost importance. Return currents passing through the plane will cause a voltage to drop across it: (2)

$$V_r = j\omega L_p$$

Where:

V_r = Voltage dropped across the return plane

ω = Frequency in radians per second = $2\pi f$

L_p = Partial inductance of the return plane

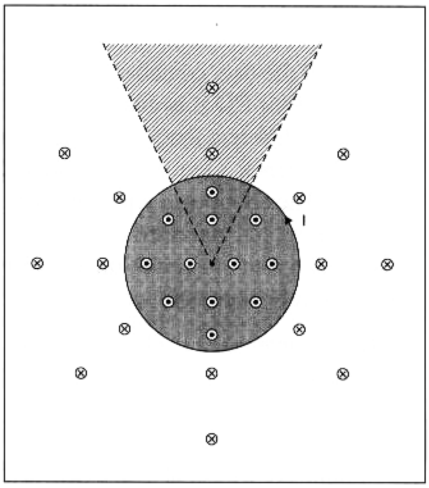

Figure 1: A loop of wire carrying current I has an inductance defined as the ratio of the magnetic flux through the loop divided by the current. Here, magnetic field lines are shown either as moving into the plane of the page (⊗) or out of it ( ). A portion of the loop can be assigned a partial inductance by calculating the flux in the crosshatched area outside the loop.

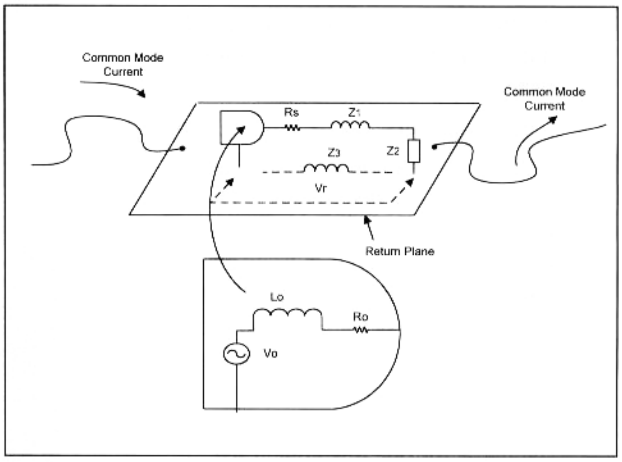

Figure 2: The return plane has a partial inductance and therefore will exhibit a voltage drop V_r across it. This voltage causes wires connected to the return, either directly or incrementally, to radiate.

The voltage, V_r, will cause wires attached to the return plane to radiate as shown in Figure 2.

As noted, partial inductance is generally defined as illustrated in Figure 1. The segment to be assigned a partial inductance is identified and then an area, either inside or outside the loop is defined corresponding to that segment. Measuring the total flux through either of these areas and dividing it by the current in the segment yields the partial inductance. Usually the area outside the loop is used.

The concept of partial inductance is useful for solving problems that would otherwise seem intractable. Take, for example, the calculation of the inductance of a single straight, infinitely long wire. In theory, only loops have inductance. Nonetheless, we have all experienced situations in which a wire seemed to have an inductance per unit length, and where the current loop itself seems to be difficult or impossible to define. Using the concept of partial inductance, however, we can use Figure 3 to calculate the drop expected per unit length of wire due to inductance. The flux through the area shown, which is defined as a surface of infinite length perpendicular to a selected segment of the wire, divided by the current in that segment yields the partial inductance.

So far we have been talking about the inductance of a single wire isolated in space. Wires however, are rarely so isolated. For example, two parallel wires are shown in Figure 4. Here, the partial inductance of our segment is due both to the flux generated by the current flowing in wire 1 and the flux generated from the current flowing in wire 2. (3)

$$L_{p\ tot} = L_{11} - L_{12}$$

Where:

$L_{p\ tot}$ = Total partial inductance of a segment of wire 1.

L_{11} = Partial inductance of wire 1 due to the flux generated by the current on wire 1.

L_{12} = Partial inductance of wire 1 due to the flux generated by the current on wire 2.

The term L_{11}, that is the ratio of the flux generated by the current flowing in wire 1

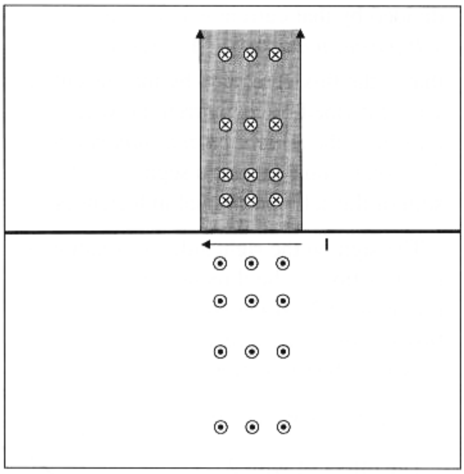

Figure 3: The partial inductance of a straight segment of wire can be calculated by taking the flux through the shaded area and dividing it by the current.

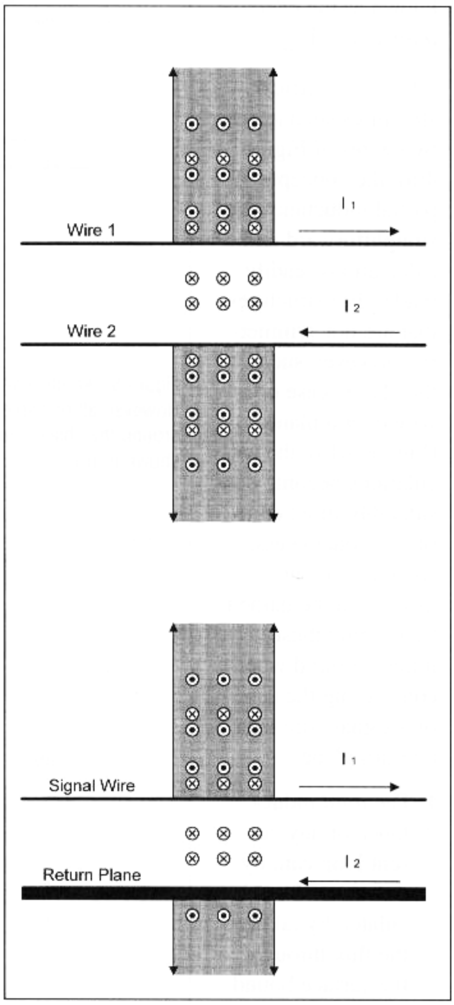

Figure 4: A pair of wires (a) carrying opposing currents will produce opposing fields in the shaded areas. The total partial inductance of the shaded segment is calculated by taking the net flux and dividing by the current. In the same manner, the partial inductance of a segment of a return plane can be calculated by taking the flux through the shaded area below the plane and dividing by the current as shown in (b).

divided by that current is known as the *self partial inductance.* The term L_{12}, that is the flux generated by the current on wire 2 divided by the current on wire 1 is known as the *mutual partial inductance.* The total inductance of a segment is the sum of the self and mutual inductances.

The sign on the right side of Equation 3 is a function of the direction of the current in wire 2. If the current in wire 2 flows in the same direction as the current in wire 1 then Equation 3 becomes: (4)

$$L_{p\,tot} = L_{11} + L_{12}$$

The effect of wire 2 is then to raise the inductance of wire 1.

$L_{p\,tot}$ is sometimes known as the *effective inductance,* L_{eff}.

For symmetrical structures such as the two wires of Figure 4(a), the concepts of partial inductance are straightforward and calculations readily made. For structures that are not symmetric, however, such as the classic case of a wire over a plane (Figure 4(b)), the calculations become considerably more complex. Nonetheless, some important insight can be gained by keeping these things in mind when considering the case of a signal wire over a return plane:

1. The *total* inductance of any current loop can, by definition, be calculated by taking the flux through the surface bounded by the loop and dividing it by the current.
2. The *partial* inductance of a portion or segment of the signal wire can be calculated by mapping a rectangular area *above* the loop formed by the signal wire and the plane as shown in Figure 4(b). Calculating the flux in this area and dividing it by the current in that segment of the signal wire yields its partial inductance.
3. The partial inductance of a portion or segment of the return plane can be calculated by identifying a rectangular area *beneath* the return plane and cal-

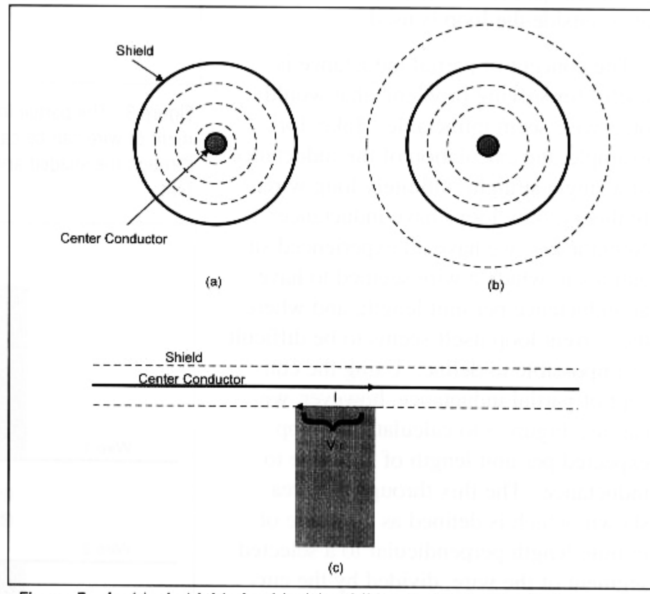

Figure 5: An ideal shielded cable (a) exhibits no return inductance. However, all real shielded cables have some flux leakage (b). The flux around the shield causes it to exhibit an inductance and a voltage drop as shown in (c).

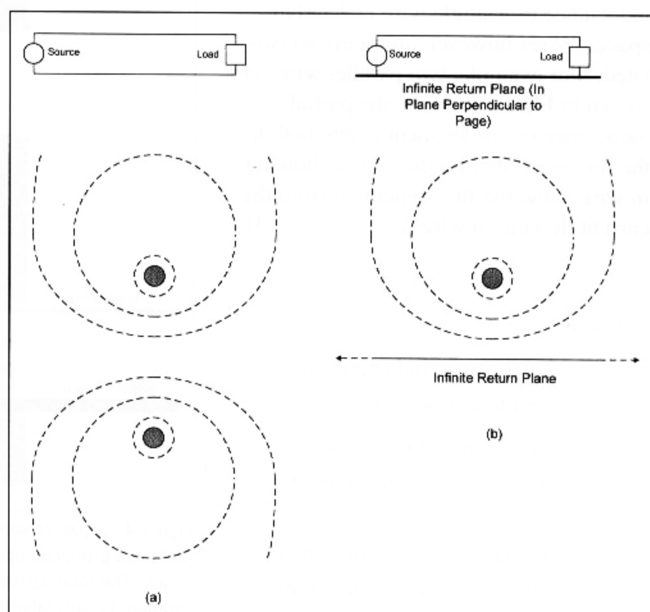

Figure 6: An open wire transmission line produces a classical dipole like magnetic field pattern as shown in (a). The pattern produced by a wire over an infinite return plane is the same (at least above the plane) as shown in (b).

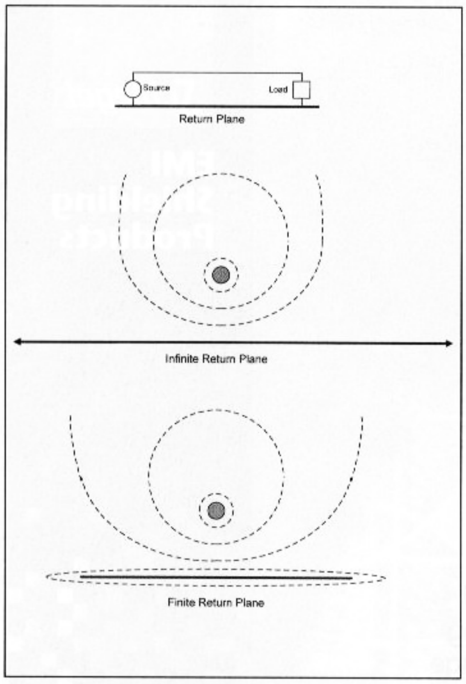

Figure 7: Real return planes are finite in size, so some flux leaks around the edges of the return plane, accounting for its partial inductance.

culating the flux through it. That, divided by the current in that segment of the return plane yields its partial inductance.

As discussed in our previous articles, the larger the return plane's partial inductance, the greater the radiation that is likely to result.

Obviously, making the return plane infinitely wide will result in a return plane partial inductance of zero. An infinitely wide return plane will prevent any magnetic field lines from passing through it and there will be no flux in the lower rectangular area of Figure 4(b).

The same is also true for an ideal shielded cable (Figure 5(a)). Here, all the magnetic field lines created by the center conductor are trapped within the shield. No flux extends beyond the shield and therefore the partial inductance of the shield is zero. All the inductance of the circuit is represented by the center conductor through the sum of its partial inductances. If all of our circuits were either ideal shielded cables or had return planes of infinite width there would be little radiation from digital devices. Our problems come about principally because practical shielded cables don't completely trap the flux internally and because practical return planes are of finite width.

Leferink, in a 1992 paper [3] introduced the concept of *lost flux*. In the case of a shielded cable any flux that is lost, that is which is due to magnetic fields around the shield rather than within it, accounts for partial inductance of the shield and will result in a voltage drop across it and associated radiation. The same concept of lost flux can be applied to the case of a wire over a plane. Fields that wrap around the plane represent "lost" flux and minimizing this "lost" flux is key to minimizing the voltage drop across the plane and associated radiation (Figure 7).

In his 1994 paper [1], Leferink tabulated the calculated partial inductances of the return conductors for various geometries. Some of these have been included in Figures 8 and 9 and in Table 1. To make things manageable, Leferink had to

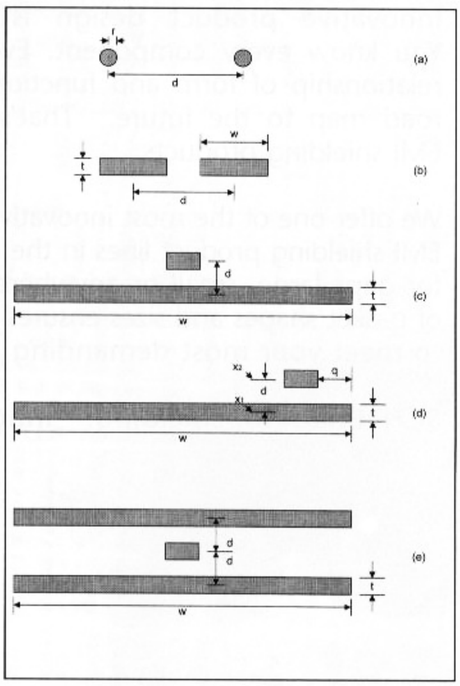

Figure 8: Some common wire geometries. The return partial inductance is tabulated for each in Table 1.

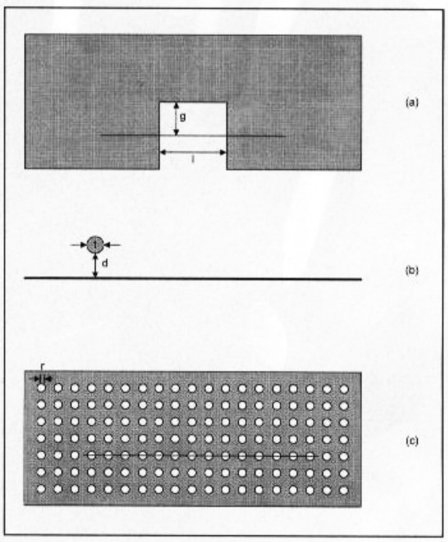

Figure 9: Gaps (a) and holes (c) can raise the return plane's impedance. Figure 9(b) is a side view of the arrangement.

Description of Circuit	Figure	L_{eff} -- Partial Inductance of the Return	Notes
Ideal Shielded Cable	Fig. 5a	$L_{eff} = 0$	Ideal Shield
Open Wire	Fig. 8a	$\frac{ul}{2\pi} \ln (\frac{d}{r} - 1)$	Wire radii equal
Traces Side by Side	Fig. 8b	$\frac{ul}{2\pi} \ln (\frac{\pi(d-w)}{w-t} + 1)$	
Microstrip	Fig. 8c	$\frac{ul}{2\pi} \frac{d}{w}$	
Offset Microstrip	Fig. 8d	$\frac{ul}{2\pi w} \int_{x1}^{x2} (atan \frac{q}{x} + atan \frac{w-q}{x}) dx$	
Stripline	Fig. 8e	$\frac{ul}{2\pi} \ln (\frac{\pi d}{w} + 1)$	t = 0
Return Plane with Gap	Fig. 9a	$L_{plane} + \frac{ul}{2\pi} \ln (\frac{g}{t})$	g > d
Return Plane with Holes	Fig. 9c	$L_{plane} + v \times \frac{\mu r^3}{3\pi^2 d^2} \times e^{-t/r}$	v = no. holes per unit length

Note: *l* in the equations above is the length of the return or a portion of the return. It does not appear in the figures. Inductances are in Henries. In terms of inductance per unit length, the term $(\mu l/2\pi)$=2nH/cm.

Table 1

limit himself to a number of assumptions. These were:

1. All of the marked dimensions in the figures are considered to be small compared to the wavelength.
2. The current distribution in the signal conductor (or to use Leferink's terminology, the flux generating conductor, FGC) is considered to be uniform.
3. The length of the transmission line formed is much greater than all the other dimensions.
4. The radius **r** where shown or the thickness **t** are considered to be equal for the signal conductor and the return conductor.

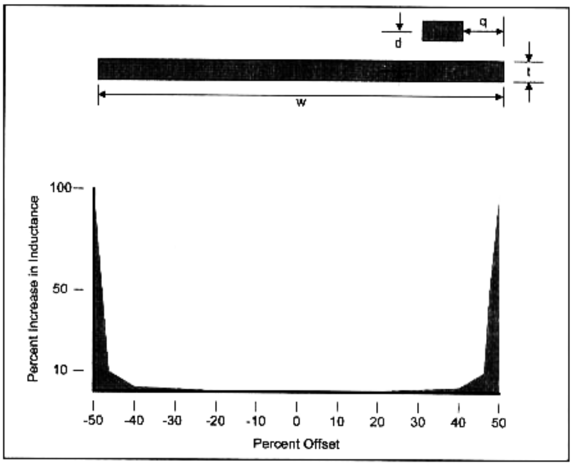

Figure 10: Moving a trace towards the edge of a board raises its inductance.

Leferink's tabulations are a most useful guide. Compare, for example, the effective return inductance of a pair of round wires versus a two traces. Further, as noted, the return inductance of a solid coaxial cable is predicted to be zero. Leferink also provides formulas for calculating the inductance due to a gap in the return plane and holes in the plane.

These formulas allow us to predict, to at least a first approximation, the inductances presented by common geometries. Take for example, a wire suspended above a plane. As we all know from our practical work, the effective inductance falls as the width of the plane becomes greater. We also can calculate the effect of moving a signal conductor closer to the edge of a plane. Here the formulas tabulated by Leferink predict that the inductance of the return plane will rise as the signal conductor gets closer to the edge of the plane. However, this rise is small until the signal conductor gets quite close to the edge (Figure 10). We also can compare the inductance of a strip line as compared to a micro strip.

Finally, we can use the formulas to predict the increase in a return plane's inductance due to holes or a gap in the return plane. For a gap whose dimensions are l=10mm, g=50mm and t=0.035mm, L_{gap}=14.5nH. For a plane studded with holes of radius 1mm and d=1.6mm, each hole over which the signal line passes will contribute 17 pH. Small holes in the return plane do not tend to increase radiation markedly, though gaps do.

In our upcoming articles we will return to the laboratory to devise methods for reducing radiation which will take direct advantage of what we know about the nature of partial inductances. ■

References

1. T. Hubing, T. Van Doren and J. Drewniak, "Identifying and Quantifying Printed Circuit Board Inductance," IEEE Symposium on Electromagnetic Compatibility, 1994, Page 205.

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3. F. Leferink, "Preventing Electromagnetic Interference from Integrated Circuits and Printed Circuit Boards using Computer Simulation," Twente University of Technology, Rep. EL-BSC-92N138, 1992.